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1 Analysis of Noise Avoidance Techniques in DSM Interconnects Using a Complete Crossta

M. Becer, V. Zolotov, D. Blaauw, R. Panda, I. Hajj

March 2002 Proceedings of the conference on Design, automation and test in Europe

Publisher: IEEE Computer Society

Full text available:

pdf(277.35 KB) Publisher Site

Additional Information: full citation, abstract

Noise estimation and avoidance are becoming critical, must have' capabilities in today's high perf IC design. An accurate yet efficient crosstalk noise model which contains as many driver/interconi parameters as possible, is neccesary for any sensitivity based noise avoidanceapproach. In this p present a complete analytical crosstalk noise model which incorporates all physical properties included analytical crosstalk noise model which incorporates all physical properties included analytical crosstalk noise model which incorporates all physical properties included analytical crosstalk noise model which incorporates all physical properties included analytical crosstalk noise model which incorporates all physical properties included analytical crosstalk noise model which incorporates all physical properties included analytical crosstalk noise model which incorporates all physical properties included analytical crosstalk noise model which incorporates all physical properties included analytical cross-table analytical cr victim and aggressor drivers, distributed RCcharacteristics of interconnects and coupli ...

<sup>2</sup> Improved crosstalk modeling for noise constrained interconnect optimization

Jason Cong, David Zhigang Pan, Prasanna V. Srinivas

January 2001 Proceedings of the 2001 conference on Asia South Pacific design automation

Publisher: ACM Press

Full text available: pdf(158.23 KB)

Additional Information: full citation, abstract, references, citings, index terr

This paper presents a much improved, highly accurate yet efficient crosstalk noise model, the 2model, and applies it to noise-constrained interconnect optimizations. Compared with previous c noise models of similar complexity, our 2-pie model takes into consideration many key paramete as coupling locations (near-driver or near-receiver), and the coarse distributed RC characteristic victim net. Thus, it is very accurate (less than 6% error on average compared with H ...

3 <u>Driver modeling and alignment for worst-case delay noise</u>

Supamas Sirichotiyakul, David Blaauw, Chanhee Oh, Rafi Levy, Vladimir Zolotov, Jingyan Zuo June 2001 Proceedings of the 38th conference on Design automation

Publisher: ACM Press

Full text available: pdf(895.48 KB)

Additional Information: full citation, abstract, references, citings, index terr

In this paper, we present a new approach to model the impact of cross-coupling noise on interco delay. We introduce a new linear driver model that accurately models the noise pulse induced or switching signal net due to cross coupling capacitance. The proposed model effectively captures linear behavior of the victim driver gate during the transition and has an average error below 89 the traditional approach using a Thevenin model incurs an average error of 48% ...

### 4 Crosstalk noise analysis: A simplified transmission-line based crosstalk noise model for on **RLC** wiring

Kanak Agarwal, Dennis Sylvester, David Blaauw

January 2004 Proceedings of the 2004 conference on Asia South Pacific design automation electronic design and solution fair ASP-DAC '04, Proceedings of the 2004 col on Asia South Pacific design automation: electronic design and solution fair / '04

Publisher: IEEE Press, IEEE Press

Full text available: pdf(232.14 KB) Publisher Site

Additional Information: full citation, abstract, references

In this paper, we present a new RLC crosstalk noise model that combines simplicity, accuracy, a generality. The new model is based on transmission line theory and is applicable to asymmetric line configurations. The results show that the model captures both the waveform shape and peal accurately (average error in peak noise was 6.5%). A key feature of the new model is that its de and form enables physical insight into the dependency of total coupling noise on relevant ...

## Efficient crosstalk noise modeling using aggressor and tree reductions

Li Ding, David Blaauw, Pinaki Mazumder

November 2002 Proceedings of the 2002 IEEE/ACM international conference on Computer-

Publisher: ACM Press

Full text available: pdf(139.91 KB)

Additional Information: full citation, abstract, references, index terms

This paper describes a fast method to estimate crosstalk noise in the presence of multiple aggrefor use in physical design automation tools. Since noise estimation is often part of the innerloop optimization algorithms, very efficient closed-form solutions are needed. Previous approaches he typically used simple lumped 3--4 node circuit templates. One aggressor net is modeled at a tim assuming that the coupling capacitances to all quiet aggressor nets are grounded. They also move

6 Poster session 1: Noise aware behavioral modeling of the E-Δ fractional-N frequency synth

Lei Yang, Cherry Wakayama, C.-J. Richard Shi

April 2005 Proceedings of the 15th ACM Great Lakes symposium on VLSI

Publisher: ACM Press

Full text available: pdf(259.26 KB)

Additional Information: full citation, abstract, references, index terms

This paper presents the behavioral model of a  $E-\Delta$  fractional-N frequency synthesizer in terms of noise sources and non-ideal effects. To accurately predict the phase noise of the synthesizer, dif jitter noise sources such as phase modulation (PM) noise in phase-frequency detector and divide frequency modulation (FM) noise in VCO are properly depicted. The E-Δ modulator, with its divic dithered and quantization noise dynamically injected to the PLL, i ...

Keywords: PLL, frequency synthesizer, jitter noise, phase noise

#### Substrate Noise Analysis with Compact Digital Noise Injection and Substrate Models Makoto Nagata, Youichi Nishimori, Takashi Morie, Atsushi Iwata, Yoshitaka Murasaka January 2002 Proceedings of the 2002 conference on Asia South Pacific design automation Design

Publisher: IEEE Computer Society

Full text available: pdf(512.69 KB) Publisher Site

Additional Information: full citation, abstract

This paper presents a substrate noise analysis methodology that employs chip-level substrate m based on F-matrix computation and digital substrate-noise injection modeling with a time-series

parasitic capacitance model for time-domain power-supply current estimation. System-level simu models generated accordingly to the methodology provide reliable substrate noise waveforms. Si waveforms for practical digital circuits on a 0.6-um CMOS 4.5-mm square chip are well consist.

8 Noise-tolerant learning, the parity problem, and the statistical query model

Avrim Blum, Adam Kalai, Hal Wasserman
July 2003 Journal of the ACM (JACM)

Journal of the ACM (JACM), Volume 50 Issue 4

**Publisher: ACM Press** 

Full text available: pdf(132.90 KB) Additional Information: full citation, abstract, references, index terms

We describe a slightly subexponential time algorithm for learning parity functions in the presencrandom classification noise, a problem closely related to several cryptographic and coding proble algorithm runs in polynomial time for the case of parity functions that depend on only the first O log n) bits of input, which provides the first known instance of an efficient noise-tolerant algorith concept class that is not learnable in the Statistical ...

Keywords: Computational learning theory, machine learning, statistical queries

<sup>9</sup> A noise model on learning sets of strings

Yasubumi Sakakibara, Rani Siromoney
July 1992 Proceedings of the fifth

Proceedings of the fifth annual workshop on Computational learning theory

Publisher: ACM Press

Full text available: pdf(714.91 KB)

Additional Information: full citation, abstract, references, citings, index terr

In this paper, we introduce a new noise model on learning sets of strings in the framework of PA and consider the effect of the noise on learning. The instance domain is the set &Sgr;n of strings finite alphabet &Sgr;, and the examples are corrupted by purely random errors affecting only the instances (and not the labels). We consider three types of errors on instances, called EDIT opera errors. EDIT operations cons ...

10 Modeling and Evaluation of Substrate Noise Induced by Interconnects

Ferran Martorell, Diego Mateo, Xavier Aragones

March 2003 Proceedings of the conference on Design, Automation and Test in Europe - Vol **DATE '03** 

Publisher: IEEE Computer Society Full text available: pdf(263.32 KB)

Publisher Site

Additional Information: full citation, abstract, index terms

Interconnects have deserved attention as a source of crosstalk to other interconnects, but have ignored as a source of substrate noise. In this paper, we evaluate the importance of interconnec substrate noise. A known interconnect and substrate model is validated by comparing simulation experimental measurements. Based on the validated modeling approach, a complete study cons frequency, geometrical, load and shielding effects is presented. The importance of interc ...

11 Symbolic circuit-noise analysis and modeling with determinant decision diagrams

XiangDong Tan, C.-J. Richard Shi

January 2000 Proceedings of the 2000 conference on Asia South Pacific design automation

Publisher: ACM Press

Full text available: pdf(226.93 KB)

Additional Information: full citation, references

12 Accurate Estimating Simultaneous Switching Noises by Using Application Specific Device L. Ding, P. Mazumder

March 2002 Proceedings of the conference on Design, automation and test in Europe

Publisher: IEEE Computer Society Full text available: pdf(215.61 KB)

Publisher Site

Additional Information: full citation, abstract

In this paper, we study the simultaneous switching noiseproblem by using an application-specific method. A simple yet accurate MOSFET model is proposed in orderto derive closed-form formula: simultaneous switchingnoise voltage waveforms. We first derive a simple formulaassuming that inductances are the only parasitics. Andthrough HSPICE simulation, we show that the new formu accurate than previous results based on the sameassumption. We then study the effect of the page 1

### 13 Crosstalk noise analysis: A non-iterative model for switching window computation with cros noise

Janet Meiling Wang, Omar Hafiz, Pinhong Chen

January 2004 Proceedings of the 2004 conference on Asia South Pacific design automation electronic design and solution fair ASP-DAC '04, Proceedings of the 2004 col on Asia South Pacific design automation: electronic design and solution fair I '04

Publisher: IEEE Press, IEEE Press Full text available: pdf(268.27 KB)

Publisher Site

Additional Information: full citation, abstract, references

Proper modeling of the switching windows leads to a better estimate of the noise induced delay. The present paper proposes a new continous switching window model. This new model is combir an ordering technique that avoids convergence and multiple solution issues in the fixed point ite methods. Experimental results show that our new model can achieve 2-3x times speedup over the point iteration methods, and provide better simulation results than the discrete models an ...

## 14 Modeling Noise Transfer Characteristic of Dynamic Logic Gates

Li Ding, Pinaki Mazumder

March 2003 Proceedings of the conference on Design, Automation and Test in Europe - Vol **DATE '03** 

Publisher: IEEE Computer Society

Publisher Site

Full text available: pdf(118.99 KB)

Additional Information: full citation, abstract, index terms

Dynamic noise analysis is recently gaining more attention as a definitive method to overcome ql. deficiencies of static noise analysis. Exact dynamic noise analysis requires modeling of both injection and propagated noise. In this paper, we have developed a strategy to study the noise propagation problem. An efficient analytical formula has been derived to accurately model the noise waveform characteristic of dynamic CMOS logic gates. Experiments have shown that the maximum err ...

#### <sup>15</sup> Modeling for analog circuits: High-frequency noise in RF active CMOS mixers Payam Heydari

January 2004 Proceedings of the 2004 conference on Asia South Pacific design automation electronic design and solution fair ASP-DAC '04, Proceedings of the 2004 cou on Asia South Pacific design automation: electronic design and solution fair / '04

Publisher: IEEE Press, IEEE Press

Full text available: pdf(188.90 KB) Publisher Site

Additional Information: full citation, abstract, references

A new analytical model for high-frequency noise in RF active CMOS mixers such as single-balanc double-balanced architectures is presnted. The analysis includes the contribution of non-white qu induced noise at the output as well as the spot noise figure (NF) of the RF CMOS mixer, while ac for the non-zero correlation between the gate-induced noise and the channel thermal noise. The

contribution of the RF transconductor as well as the switching pair on the output noise is di ...

Modeling crosstalk noise for deep submicron verification tools

P. Bazargan-Sabet, F. Ilponse

March 2001 Proceedings of the conference on Design, automation and test in Europe

Publisher: IEEE Press

Full text available: pdf(81.94 KB)

Additional Information: full citation, references, index terms

### 17 <u>EM Wave Coupling Noise Modeling Based on Chebyshev Approximation and Exact Mome</u> Formulation

Baohua Wang, Pinaki Mazumder

March 2005 Proceedings of the conference on Design, Automation and Test in Europe - Vol

Publisher: IEEE Computer Society

Full text available: pdf(310.59 KB)

Additional Information: full citation, abstract

This paper presents a new mathematical approach to modeling EM wave coupling noise so that i easily integrated into chip-level noise analysis tools. The new method employs Chebyshev approtechnique to model the distributed sources arising in the Telegrapher's equations due to EM wave coupling. A uniform plane wave illumination metric is provided to determine the order of approxic Closed-form formulas for the noise transfer functions' moments are derived. By utilizing the four contents are derived.

## 18 Delay and noise modeling in the nanometer regime: Non-iterative switching window compt

delay-noise

Bhavana Thudi, David Blaauw

June 2003 Proceedings of the 40th conference on Design automation

Publisher: ACM Press

Full text available: pdf(138.38 KB)

Additional Information: full citation, abstract, references, citings, index terr

In this paper, we present an efficient method for computing switching windows in the presence  $\mathfrak{c}$  noise. In static timing analysis, delay noise has traditionally been modeled using a simple switch based noise model and the computation of switching windows is performed using an iterative algresulting in an overall run time of O(n2), where n is the number of gates in the circuit. It has als shown that the iterations converge to different solutions, depending on the initia ...

**Keywords**: cross-talk noise, superposition, switching window

## Noise-tolerant learning, the parity problem, and the statistical query model

Avrim Blum, Adam Kalai, Hal Wasserman

May 2000 Proceedings of the thirty-second annual ACM symposium on Theory of computi

Publisher: ACM Press

Full text available: pdf(673.02 KB)

Additional Information: full citation, references, citings, index terms

# 20 Analog circuit design: Substrate noise modeling in early floorplanning of MS-SOCs

Grzegorz Blakiewicz, Marcin Jeske, Malgorzata Chrzanowska-Jeske, Jin S. Zhang
January 2005 Proceedings of the 2005 conference on Asia South Pacific design automation
DAC '05

Publisher: ACM Press

Full text available: pdf(498.14 KB)

Additional Information: full citation, abstract, references

We propose a frequency-dependent sensitivity model for analog blocks and a noise injection modeligital blocks in application to early design planning of Mixed-Signal System-on-Chips (MS-SOCs

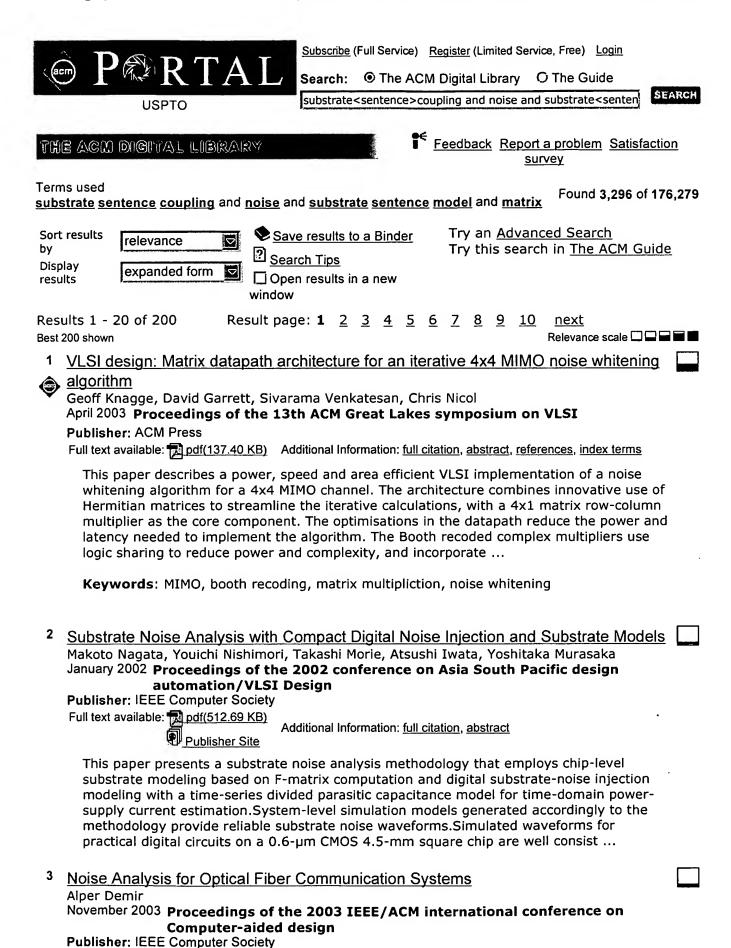
assume no precise layout information about IP cores is available. We also propose an empirical f for separation-dependent coupling between large-area noisy ports and small-area sensitive ports lightly-doped substrates that are preferred for mixed-signal circuits. The interaction between ...

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	The optical fiber transmission links form the backbone of the communicationsinfrastructure. Almost all of voice and data (internet) traffic is routed throughterrestrial and submarine optical fiber links, connecting the world together. Invention of the optical amplifiers (OAs) and wavelength-division multiplexing(WDM) technology enabled very high capacity optical fiber communicationlinks that run for thousands of kilometers without any electronic repeaters, but the same time brought many design	
4	Traffic engineering: An information-theoretic approach to traffic matrix estimation Yin Zhang, Matthew Roughan, Carsten Lund, David Donoho August 2003 Proceedings of the 2003 conference on Applications, technologies, architectures, and protocols for computer communications Publisher: ACM Press	
	Full text available: pdf(421.04 KB)  Additional Information: full citation, abstract, references, citings, index terms	
	Traffic matrices are required inputs for many IP network management tasks: for instance, capacity planning, traffic engineering and network reliability analysis. However, it is difficult to measure these matrices directly, and so there has been recent interest in inferring traffic matrices from link measurements and other more easily measured data. Typically, this inference problem is ill-posed, as it involves significantly more unknowns than data. Experience in many scientific and engineering f	
	<b>Keywords</b> : SNMP, information theory, minimum, mutual information, regularization, traffic engineering, traffic matrix estimation	
5 �	Phase noise in oscillators: DAEs and colored noise sources Alper Demir November 1998 Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design	
	Publisher: ACM Press Full text available: pdf(869.85 KB) Additional Information: full citation, references, citings, index terms	
6	Global harmony: coupled noise analysis for full-chip RC interconnect networks K. L. Shepard, V. Narayanan, P. C. Elmendorf, Gutuan Zheng November 1997 Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design Publisher: IEEE Computer Society	
	Full text available: pdf(238.78 KB) Additional Information: full citation, abstract, references, citings, index terms	
	Noise is becoming one of the most important metrics in the design of VLSI systems, certainly of comparable importance to area, timing, and power. In this paper, we describe Global Harmony, a methodology for the analysis of coupling noise in the global interconnect of large VLSI chips, being developed for the design of high-performance microprocessors. The architecture of Global Harmony involves a careful combination of static noise analysis, static timing analysis, and reduced-order modelling te	
	Keywords: noise, static timing analysis, interconnect	
7	Noise Macromodel for Radio Frequency Integrated Circuits	

Yang Xu, Xin Li, Peng Li, Lawrence Pileggi March 2003 Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '03 Publisher: IEEE Computer Society Full text available: pdf(216.67 KB) Additional Information: full citation, abstract, index terms Publisher Site Noise performance is a critical analog and RF circuit design constraint, and can impact the selection of the IC system-level architecture. It is therefore imperative that some model of the noise is represented at the highest levels of abstraction during the design process. In this paper we propose a noise macromodel for analog circuits and demonstrate it by way of implementation in a system level simulator based on MATLAB. We also explain our process of macromodel extraction via reformulation of ... 8 Power and noise: Noise driven in-package decoupling capacitor optimization for power integrity Jun Chen, Lei He April 2006 Proceedings of the 2006 international symposium on Physical design ISPD Publisher: ACM Press Full text available: pdf(164.11 KB) Additional Information: full citation, abstract, references, index terms The existing decoupling capacitance optimization approaches meet constraints on input impedance for package. In this paper, we show that using impedance as constraints leads to large overdesign and then develop a noise driven optimization algorithm for decoupling capacitors in packages for power integrity. Our algorithm uses the simulated annealing algorithm to minimize the total cost of decoupling capacitors under the constraints of a worst case noise. The key enabler for efficient optimization ... Keywords: IC package, decoupling capacitor, integrity, modeling, noise, power, power distribution system, resonance 9 <u>Time-domain non-Monte Carlo noise simulation for nonlinear dynamic circuits with</u> arbitrary excitations Alper Demir, Edward W. Y. Liu, Alberto L. Sangiovanni-Vincentelli November 1994 Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design Publisher: IEEE Computer Society Press Additional Information: full citation, abstract, references, citings, index Full text available: pdf(840.83 KB) terms A new, time-domain, non-Monte Carlo method for computer simulation of electrical noise in nonlinear dynamic circuits with arbitrary excitations is presented. This time-domain noise simulation method is based on the results from the theory of stochastic differential equations. The noise simulation method is general in the sense that any nonlinear dynamic circuit with any kind of exci ... 10 Session 9A: noise and performance issues in routing: A twisted-bundle layout structure for minimizing inductive coupling noise Guoan Zhong, Cheng Kok Koh, Kaushik Roy November 2000 Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design Publisher: IEEE Press Full text available: pdf(105.24 KB) Additional Information: full citation, abstract, references, citings In this paper, we propose a novel twisted-bundle layout structure for minimizing inductive

coupling noise. In this structure, we create several routing regions and re-order the routing of nets in each of these routing regions. The purpose is to create complementary and opposite current loops in the twisted-bundle layout structure, such that the magnetic fluxes arising from any signal net within a *twisted group* cancel each other in the current loop of a net of interest. The effectiv ...

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11	n: Computing phase noise eigenfunctions natrices wdhury DO IEEE/ACM international conference on n al Information: full citation, abstract, references, citings
	se calculation lies in computing a vector function for (PPV). Current techniques for PPV calculation use system's monodromy matrix, followed by full or perior method that finds the PPV using only a single or frequency-domain steady-state Jacobian matrix.
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13	eclercq 22 IEEE/ACM international conference on  Il Information: full citation, abstract, references, index terms of integration of RF, analog and digital blocks results at can degrade performance and hence, should be a practical methodology that uses a suite of a high-speed extractor based on an innovative semi-purling problems, and enable RF designers to
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Noise reduction in a statistical approach to text categorization

<b>\$</b>	Yiming Yang July 1995 Proceedings of the 18th annual international ACM SIGIR conference on Research and development in information retrieval Publisher: ACM Press Full text available: pdf(895.10 KB) Additional Information: full citation, references, citings, index terms	
15	Circuit noise evaluation by Padé approximation based model-reduction techniques Peter Feldmann, Roland W. Freund November 1997 Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design Publisher: IEEE Computer Society Full text available: pdf(484.17 KB) Additional Information: full citation, abstract, references, citings, index terms  This paper introduces a new circuit noise analysis and modeling method. The noise analysis method computes an analytic expression of frequency, in rational form, which represents the Pad\'e approximation of the noise power spectral density. The approximation can be carried out efficiently, to the required accuracy, using a variant of the PVL~\cite{FeIF95} or MPVL~\cite{FeIF95b} algorithms. The new method is significantly more efficient than traditional methods for noise computation at numerous f  Keywords: circuit simulation, noise analysis, reduced-order modeling, Pade approximation, Lanczos process	
16 <b>②</b>	Emolent 7 to drie holde drianysis of two-tone fit circuits	
17	Noise-tolerant learning, the parity problem, and the statistical query model  Avrim Blum, Adam Kalai, Hal Wasserman  July 2003 Journal of the ACM (JACM), Volume 50 Issue 4  Publisher: ACM Press  Full text available: pdf(132.90 KB) Additional Information: full citation, abstract, references, index terms  We describe a slightly subexponential time algorithm for learning parity functions in the presence of random classification noise, a problem closely related to several cryptographic and coding problems. Our algorithm runs in polynomial time for the case of parity functions that depend on only the first O(log n log log n) bits of input, which provides the first known instance of an efficient noise-tolerant algorithm for a concept class that is not learnable in the Statistical  Keywords: Computational learning theory, machine learning, statistical queries	
	Shared resource matrix methodology: an approach to identifying storage and timing channels Richard A. Kemmerer August 1983 ACM Transactions on Computer Systems (TOCS). Volume 1 Issue 3	

Results (page 1): substrate<sentence>coupling and noise and substrate<sentence>model\* ... Page 6 of 6 Publisher: ACM Press Full text available: pdf(1.27 MB) Additional Information: full citation, references, citings, index terms **Keywords**: confinement, covert channels, flow analysis, protection, storage channels, timing channels, validation 19 Memory Matrix Using Ferroelectric Condensers as Bistable Elements Charles F. Pulvari July 1955 Journal of the ACM (JACM), Volume 2 Issue 3 Publisher: ACM Press Full text available: pdf(2.36 MB) Additional Information: full citation, references, index terms 20 Crosstalk noise avoidance and power/ground network optimization: Successive pad assignment algorithm to optimize number and location of power supply pad using incremental matrix inversion Takashi Sato, Masanori Hashimoto, Hidetoshi Onodera January 2005 Proceedings of the 2005 conference on Asia South Pacific design automation ASP-DAC '05 Publisher: ACM Press Full text available: pdf(748.73 KB) Additional Information: full citation, abstract, references An efficient pad assignment algorithm to minimize voltage drop on a power distribution network is proposed. Combination of the successive pad assignment (SPA) and the incremental matrix inversion (IMI) provides an efficient assignment for both location and number of power supply pads. The SPA creates equivalent resistance matrix which preserves both pad candidates and power consumption points as external ports so that topological modification due to connection or disconnection between voltage so ...

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Substrate Noise Analysis with Compact Digital Noise Injection and Substrate Models

Makoto Nagata, Youichi Nishimori, Takashi Morie, Atsushi Iwata, Yoshitaka Murasaka January 2002 Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design

Publisher: IEEE Computer Society Full text available: pdf(512.69 KB)

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Additional Information: full citation, abstract

This paper presents a substrate noise analysis methodology that employs chip-level substrate modeling based on F-matrix computation and digital substrate-noise injection modeling with a time-series divided parasitic capacitance model for time-domain powersupply current estimation. System-level simulation models generated accordingly to the methodology provide reliable substrate noise waveforms. Simulated waveforms for practical digital circuits on a 0.6-µm CMOS 4.5-mm square chip are well consist ...

<sup>2</sup> Noise-tolerant learning, the parity problem, and the statistical query model



Avrim Blum, Adam Kalai, Hal Wasserman

July 2003 Journal of the ACM (JACM), Volume 50 Issue 4

Publisher: ACM Press

Full text available: pdf(132.90 KB) Additional Information: full citation, abstract, references, index terms

We describe a slightly subexponential time algorithm for learning parity functions in the presence of random classification noise, a problem closely related to several cryptographic and coding problems. Our algorithm runs in polynomial time for the case of parity functions that depend on only the first  $O(\log n \log \log n)$  bits of input, which provides the first known instance of an efficient noise-tolerant algorithm for a concept class that is not learnable in the Statistical ...

Keywords: Computational learning theory, machine learning, statistical queries

<u>Circuit noise evaluation by Padé approximation based model-reduction techniques</u> Peter Feldmann, Roland W. Freund

http://portal.acm.org/results.cfm?coll=ACM&dl=ACM&CFID=71999810&CFTOKEN=432...

November 1997 Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design

Publisher: IEEE Computer Society

Full text available: 🔂 pdf(484.17 KB) Additional Information: full citation, abstract, references, citings, index terms Publisher Site

This paper introduces a new circuit noise analysis and modeling method. The noise analysis method computes an analytic expression of frequency, in rational form, which represents the Pad\'e approximation of the noise power spectral density. The approximation can be carried out efficiently, to the required accuracy, using a variant of the PVL~\cite{FelF95} or MPVL~\cite{FelF95b} algorithms. The new method is significantly more efficient than traditional methods for noise computation at numerous f ...

Keywords: circuit simulation, noise analysis, reduced-order modeling, Pade approximation, Lanczos process

4 Noise-tolerant learning, the parity problem, and the statistical query model

Avrim Blum, Adam Kalai, Hal Wasserman

May 2000 Proceedings of the thirty-second annual ACM symposium on Theory of computing

Publisher: ACM Press

Full text available: pdf(673.02 KB) Additional Information: full citation, references, citings, index terms

Multiple-view geometry for image-based modeling Jana Košecká, Yi Ma, Stefano Soatto, René Vidal

August 2004 Proceedings of the conference on SIGGRAPH 2004 course notes GRAPH

Publisher: ACM Press

Full text available: pdf(23.14 MB) Additional Information: full citation, abstract

This course presents the state of the art in multiple-view geometry, including methods and algorithms for reconstructing 3-D geometric models of scenes from video or photographs. This course is based on a novel approach to multiple-view geometry that only requires linear algebra, as opposed to more involved projective and algebraic geometry that most current methods employ. This new approach aims to make image-based modeling techniques accessible to a larger audience compared to existing ones. T ...

6 Estimation of parameters and eigenmodes of multivariate autoregressive models

Arnold Neumaier, Tapio Schneider

March 2001 ACM Transactions on Mathematical Software (TOMS), Volume 27 Issue 1

Publisher: ACM Press

Full text available: pdf(195.87 KB)

Additional Information: full citation, abstract, references, citings, index terms

Dynamical characteristics of a complex system can often be inferred from analysis of a stochastic time series model fitted to observations of the system. Oscillations in geophysical systems, for example, are sometimes characterized by principal oscillation patterns, eigenmodes of estimated autoregressive (AR) models of first order. This paper describes the estimation of eigenmodes of AR models of arbitrary order. AR processes of any order can be decomposed into eigenmodes with characteristi ...

7 Traffic engineering: An information-theoretic approach to traffic matrix estimation Yin Zhang, Matthew Roughan, Carsten Lund, David Donoho

August 2003 Proceedings of the 2003 conference on Applications, technologies, architectures, and protocols for computer communications

Publisher: ACM Press

Full text available: pdf(421.04 KB) Additional Information: full citation, abstract, references, citings, index terms

Traffic matrices are required inputs for many IP network management tasks: for instance, capacity planning, traffic engineering and network reliability analysis. However, it is difficult to measure these matrices directly, and so there has been recent interest in inferring traffic matrices from link measurements and other more easily measured data. Typically, this inference problem is ill-posed, as it involves significantly more unknowns than data. Experience in many scientific and engineering f ...

**Keywords**: SNMP, information theory, minimum, mutual information, regularization, traffic engineering, traffic matrix estimation

8 Symbolic circuit-noise analysis and modeling with determinant decision diagrams

XiangDong Tan, C.-J. Richard Shi

January 2000 Proceedings of the 2000 conference on Asia South Pacific design automation

Publisher: ACM Press

Full text available: pdf(226.93 KB) Additional Information: full citation, references

Global harmony: coupled noise analysis for full-chip RC interconnect networks
 K. L. Shepard, V. Narayanan, P. C. Elmendorf, Gutuan Zheng

November 1997 Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design

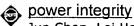
Publisher: IEEE Computer Society

Full text available: pdf(238.78 KB) Additional Information: full citation, abstract, references, citings, index terms

Noise is becoming one of the most important metrics in the design of VLSI systems, certainly of comparable importance to area, timing, and power. In this paper, we describe Global Harmony, a methodology for the analysis of coupling noise in the global interconnect of large VLSI chips, being developed for the design of high-performance microprocessors. The architecture of Global Harmony involves a careful combination of static noise analysis, static timing analysis, and reduced-order modelling te ...

**Keywords**: noise, static timing analysis, interconnect

10 Power and noise: Noise driven in-package decoupling capacitor optimization for



Jun Chen, Lei He

April 2006 Proceedings of the 2006 international symposium on Physical design ISPD '06

Publisher: ACM Press

Full text available: pdf(164.11 KB) Additional Information: full citation, abstract, references, index terms

The existing decoupling capacitance optimization approaches meet constraints on input impedance for package. In this paper, we show that using impedance as constraints leads to large overdesign and then develop a noise driven optimization algorithm for decoupling capacitors in packages for power integrity. Our algorithm uses the simulated annealing algorithm to minimize the total cost of decoupling capacitors under the constraints of a worst case noise. The key enabler for efficient optimization ...

Keywords: IC package, decoupling capacitor, integrity, modeling, noise, power, power

distribution system, resonance

## 11 Noise Macromodel for Radio Frequency Integrated Circuits

Yang Xu, Xin Li, Peng Li, Lawrence Pileggi

March 2003 Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '03

Publisher: IEEE Computer Society

Full text available: pdf(216.67 KB)

Additional Information: full citation, abstract, index terms

Publisher Site Noise performance is a critical analog and RF circuit design constraint, and can impact the selection of the IC system-level architecture. It is therefore imperative that some model of

the noise is represented at the highest levels of abstraction during the design process. In this paper we propose a noise macromodel for analog circuits and demonstrate it by way of implementation in a system level simulator based on MATLAB. We also explain our process of macromodel extraction via reformulation of ...

12 <u>Time-domain non-Monte Carlo noise simulation for nonlinear dynamic circuits with</u>

arbitrary excitations Alper Demir, Edward W. Y. Liu, Alberto L. Sangiovanni-Vincentelli

November 1994 Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design

Publisher: IEEE Computer Society Press

Additional Information: full citation, abstract, references, citings, index Full text available: pdf(840.83 KB) terms

A new, time-domain, non-Monte Carlo method for computer simulation of electrical noise in nonlinear dynamic circuits with arbitrary excitations is presented. This time-domain noise simulation method is based on the results from the theory of stochastic differential equations. The noise simulation method is general in the sense that any nonlinear dynamic circuit with any kind of exci ...

13 Coupled noise estimation for distributed RC interconnect model

Janet M. Wang, Qingjian Yu, Ernest S. Kuh

January 1999 Proceedings of the conference on Design, automation and test in Europe

**Publisher: ACM Press** 

Full text available: pdf(170.65 KB) Additional Information: full citation, index terms

14 Modeling and simulation of the interference due to digital switching in mixed-signal

Alper Demir, Peter Feldmann

November 1999 Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design

Publisher: IEEE Press

Additional Information: full citation, abstract, references, citings, index Full text available: pdf(209.73 KB)

The paper introduces a methodology for the evaluation of the interference noise, caused by digital switching activity, in sensitive circuits of a mixed-digital-analog chip. The digital switching activity is modeled stochastically as functions defined on Markov chains. The actual interference signal is obtained through the modulation of this discrete stochastic signal with real current injection patterns stored a priori in a pre-characterized library. The interference noise results from the ...







15 Session 6C: Markovian analysis and asynchronous circuits: Modeling and analysis of communication circuit performance using Markov chains and efficient graph

<u>representations</u>

Alper Demir, Peter Feldmann

November 2000 Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design

Publisher: IEEE Press

Full text available: pdf(203.08 KB) Additional Information: full citation, abstract, references

In high-speed data networks, the bit-error-rate specification on the system can be very stringent, i.e., 10-14. At such error rates, it is not feasible to evaluate the performance of a design using straightforward, simulation based, approaches. Nevertheless performance prediction before actual hardware is built is essential for the design process. This work introduces a stochastic model and an analysis-based, non-Monte-Carlo method for performance evaluation of digital data communicati ...

16 Stable and efficient reduction of substrate model networks using congruence transforms



Kevin J. Kerns, Ivan L. Wemple, Andrew T. Yang

December 1995 Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design

Publisher: IEEE Computer Society

Full text available: pdf(143.55 KB) Additional Information: full citation, abstract, references, citings, index Publisher Site

Parasitic analog-digital noise coupling has been identified as a key issue facing designers of mixed-signal integrated circuits. In particular, signal cross talk through the common chip substrate has become increasingly problematic. This paper demonstrates a new methodology for developing simulation, synthesis, and verification models to analyze the global electrical behavior of the non-ideal semiconductor substrate. RC substrate network models, which are generated via a triangular discretizatio ...

Keywords: substrate noise, mixed-signal integrated circuits, voronoi tesselation, rc network reduction, stability, congruence transform, pade approximation, lanczos process

17 Analysis and optimization of substrate noise coupling in single-chip RF transceiver



**design** 

Adil Koukab, Kaustav Banerjee, Michel Declercq

November 2002 Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design

Publisher: ACM Press

Full text available: pdf(462.15 KB) Additional Information: full citation, abstract, references, index terms

The relentless move toward single chip integration of RF, analog and digital blocks results in significant noise coupling effects that can degrade performance and hence, should be controlled. In this paper, we propose a practical methodology that uses a suite of commercial tools in combination with a high-speed extractor based on an innovative semianalytical method to deal with noise coupling problems, and enable RF designers to achieve a first silicon-success of their chips. The integration of ...

18 Inductance and substrate analysis: HSpeedEx: a high-speed extractor for substrate



noise analysis in complex mixed signal SOC Adil Koukab, Catherine Dehollain, Michel Declercq

June 2002 Proceedings of the 39th conference on Design automation

Publisher: ACM Press

Additional Information: full citation, abstract, references, citings, index Full text available: pdf(289.07 KB) terms

The unprecedented impact of noise coupling on Mixed-Signal Systems-On-a-Chip (MS-SOC) functionality, brings a new set of challenges for Electronics Design Automation (EDA) tool developers. In this paper, we propose a new approach which combines a thorough physical comprehension of the noise coupling effects with an improved Boundary-Element-Method (BEM) to accelerate the substrate model extraction and to avoid the dense matrix storage. The low computational efforts required, as well as speed and ...

**Keywords**: boundary-element-method, mixed-signal noise, noise, numerical analysis, substrate coupling, substrate noise, supply noise, switching circuits

19 Image Models

Narendra Ahuja, B. J. Schachter

December 1981 ACM Computing Surveys (CSUR), Volume 13 Issue 4

Publisher: ACM Press

Full text available: pdf(2.99 MB) Additional Information: <u>full citation</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

20 Interconnect extraction: CHIME: coupled hierarchical inductance model evaluation

Satrajit Gupta, Lawrence T. Pileggi

June 2004 Proceedings of the 41st annual conference on Design automation

Publisher: ACM Press

Full text available: 🔂 pdf(167.77 KB) Additional Information: full citation, abstract, references, index terms

Modeling inductive effects accurately and efficiently is a critical necessity for design verification of high performance integrated systems. While several techniques have been suggested to address this problem, they are mostly based on sparsification schemes for the L or L-inverse matrix. In this paper, we introduce CHIME, a methodology for non-local inductance modeling and simulation. CHIME is based on a hierarchical model of inductance that accounts for all inductive couplings at a linear cos ...

Keywords: circuit simulation, inductance modeling

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